AMENDMENTS TO THE CLAIMS

Claims 1-32. (Canceled)

Claim 33. (new) A method for testing a plurality of integrated circuits, including the steps of:

performing a plurality of tests on the plurality of integrated circuits, each of said integrated circuits having a unique identifier stored in a machine readable device;

identifying integrated circuits that failed at least one of the plurality of tests by reading said unique identifier and identifying tests failed by the integrated circuits; and

for each of said plurality of integrated circuits which has failed at least one of the plurality of tests,

creating a set of at least one test as a function of the unique identifier of a failed chip and repeating said set of at least one test the failed chip.

Claim 34. (new) The method of claim 33, wherein said machine readable device is a set of anti-fuses and said unique identifier is read by reading said set of anti-fuses.

Claim 35. (new) The method of claim 33, wherein said machine readable device is a non-volatile memory circuit and said unique identifier is read by reading said non-volatile memory circuit.

Claim 36. (new) The method of claim 35, wherein said non-volatile memory circuit is FLASH memory circuit and said unique identifier is read by reading said FLASH memory circuit.

Claim 37. (new) The method of claim 35, wherein said non-volatile memory circuit is electrical programmable read only memory (EPROM) circuit and said unique identifier is read by reading said EPROM memory circuit.

Claim 38. (new) The method of claim 35, wherein said non-volatile memory circuit is read only memory (ROM) circuit and said unique identifier is read by reading said ROM memory circuit.

Claim 39. (new) The method of claim 33, wherein said machine readable device is a content addressable memory circuit (CAM) and said unique identifier is read by reading said CAM memory circuit.

Claim 40. (new) An apparatus for testing a plurality of integrated circuits, comprising:

means for performing a plurality of tests on the plurality of integrated circuits;

means for reading a unique identifier from each integrated circuits that failed at least one of the plurality of tests and identifying tests failed by the integrated circuits; and

means for repeating at least one identified failed test on each of the integrated circuits which failed at least one test.

Claim 41. (new) The apparatus of claim 40, wherein said means for reading comprises a circuit for reading the unique identifier from a set of anti-fuses.

Claim 42. (new) The apparatus of claim 40, wherein said means for reading comprises a circuit for reading the unique identifier from a non-volatile memory.

Claim 43. (new) The apparatus of claim 42, wherein said means for reading comprises a circuit for reading the unique identifier from a FLASH memory.

Claim 44. (new) The apparatus of claim 42, wherein said means for reading comprises a circuit for reading the unique identifier from a electrical programmable read only memory (EPROM).

Claim 45. (new) The apparatus of claim 42, wherein said means for reading comprises a circuit for reading the unique identifier from a read only memory (ROM).

Claim 46. (new) The apparatus of claim 40, wherein said means for reading comprises a circuit for reading the unique identifier from a content addressable memory (CAM).

Claim 47. (new) An apparatus for testing a plurality of integrated circuits, said apparatus comprising:

a testing device for performing a plurality of tests on said plurality of integrated circuits, each of said plurality of integrated circuits having a unique circuit identifier stored in an identification circuit; and

a processor to control said testing device, said processor identifying each of said plurality of integrated circuits that failed at least one of said plurality of tests and identifying tests failed by each of said plurality of integrated circuits,

wherein said testing device repeats at least one identified failed test on each integrated circuits that failed at least one of said plurality of tests.

Claim 48. (new) The apparatus of claim 47, wherein said identification circuit is a set of anti-fuses.

Claim 49. (new) The apparatus of claim 47, wherein said identification circuit is a non-volatile memory.

Claim 50. (new) The apparatus of claim 49, wherein said non-volatile memory is a FLASH memory.

Claim 51. (new) The apparatus of claim 49, wherein said non-volatile memory is a electrical programmable read only memory (EPROM).

Claim 52. (new) The apparatus of claim 49, wherein said non-volatile memory is a read only memory (ROM).

Claim 53. (new) The apparatus of claim 47, wherein said identification circuit is a content addressable memory (CAM).

Claim 54. (new) A system comprising:

a device tester adapted to perform a principal functional test on an integrated circuit having one or more functional circuit portions and produce principal result information indicating respective operation or failure of said one or more functional circuit portions;

a reader adapted to read an identification device on said integrated circuit so as to ascertain an identity of said integrated circuit; and

a recording medium adapted to record said identity and said result information and maintain an association therebetween.

Claim 55. (new) The system of claim 54, wherein said identification device is a set of anti-fuses.

Claim 56. (new) The system of claim 54, wherein said identification device is a non-volatile memory.

Claim 57. (new) The system of claim 56, wherein said non-volatile memory is a FLASH memory.

Claim 58. (new) The system of claim 56, wherein said non-volatile memory is a electrical programmable read only memory (EPROM).

Claim 59. (new) The system of claim 56, wherein said non-volatile memory is a read only memory (ROM).

Claim 60. (new) The system of claim 54, wherein said identification device is a content addressable memory (CAM).